REMARKS

Claims 5, 8 and 12 stand rejected under 35 U.S.C. 102(e).

Claims 11 and 13 -16 stand rejected under 35 U.S.C. 103(a)

By this amendment, claims 8, 12, 14 and 16 have been cancelled without prejudice, claims 5 and 11 have been amended, and claims 17 and 18 have been newly added. Connection ports can be found in Fig. 5, showing a connector 126 for receiving the same control signals and two scanning interfaces 127 and 128. No new matter has been introduced. Accordingly, claims 5, 11, 13, 15, 17 and 18 are presently pending. Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claim Rejections

All pending claims are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of copending Application No. 09/609,651 (*Lin, et al.*)

A terminal disclaimer will be submitted after claims 5, 11, 13, 15, 17 and 18 have been reconsidered and placed in condition for allowance. Applicant must emphasize that, according to MPEP 804.02, "the filing of a terminal disclaimer to obviate a rejection based on nonstatutory double patenting is not an admission of the propriety of the rejection, *Quad Environmental Technologies Corp. v. Union Sanitary District*, 946 F.2d 870, 20 USPQ2d 1392 (Fed. Cir. 1991)," and that "filing of a terminal disclaimer simply serves the statutory function of removing the rejection of double patenting, and raises neither a presumption nor estoppel on the merits of the rejection."

Claim 5 is rejected under U.S.C. §102(e) as being anticipated by *Kinoshita et al*. (U.S. Patent No. 6,246,385, hereinafter "*Kinoshita*")

Applicant respectfully traverses the above 35 U.S.C. §102(e) rejection of claim 5 for at least the following reasons.

The limitations of claim 5 include that "the first scanning circuit board is the same as the second scanning circuit board and each scanning circuit board has a first connection port, a second connection port and a third connection port."

Kinoshita does not teach, disclose or suggest a first scanning circuit board on one side of a LCD being the same as a second scanning circuit board on the other side of the LCD.

Examiner wrongly interprets that the first scan unit 17A and the second scan unit 17B of *Kinoshita* are the same. If the first scan unit 17A and the second scan unit 17B are the same, because that they both receive the same control signals from driver power source circuit 19 and control circuit 18, the first scan unit 17A and the second scan unit 17B must scan the scan lines 12 with the same scanning direction. However, as understood by Examiner and described in Ln. 28-40, Col. 25, *Kinoshita*, the scanning directions of the first scan unit 17A and the second scan unit 17B are opposite to each other. This understanding shows an inherent difference between the first scan unit 17A and the second scan unit 17B.

Kinoshita only teaches how to use the same LSI in Ln. 42-51, Col. 25, for the first scan unit 17A and the second scan unit 17B, but does not mention any circuit board with LSIs thereon and transmitting signals to those LSIs, and there is no mention of the limitation in claim 5 that the circuit boards in the first scan unit 17A and the second scan unit 17B are the same. This application is the first one that discloses a specially-designed circuit board for application in both the first scan unit 17A and the second scan unit 17B. Referring to Fig. 5 of the present invention, the first and second scanning circuit boards 160 and 162 are the same and each has two scanning interfaces capable of connection of scan drivers. Thus, in Fig. 6a, the first scan drivers 140a and 140b are connected to the right scanning interface of the scanning circuit boards 160, and in Fig. 6b, the second scan drivers 150a and 150b to the left scanning interface of the scanning circuit boards 162.

Furthermore, even if the first scan unit 17A and the second unit 17B were the same, *Kinoshita* still does not disclose that each of the scan units has a circuit board with three connection ports as included in claim 5. Two of these three connection ports can be scanning interfaces and the remaining one can be a connector, as included in independent claim 11 and newly-added dependent claim 17. Examiner interprets the scanning line drive circuits 17A and 17B of *Kinoshita* as the scan units claimed in this application. However, each inherent circuit board in the scanning line drive circuits 17A and 17B at most discloses two connection ports: one for connecting to drive power source 19 and control circuit 18, and the other for connecting to scanning lines 12, as shown in Fig. 1 of *Kinoshita*. There is no motivation in *Kinoshita* to have a circuit board with three connection ports. Thus, there is neither a scan unit nor a circuit board having three connection ports in *Kinoshita*. Since there is at least one limitation that cannot be

found in *Kinoshita*, we respectfully request a withdrawal of the rejection under 35 USC 102.

Claim 11 stands rejected under 35 U.S.C. 103(a) as being obvious over *Kinoshita*, in view of *Sugimoto, et al.*(U.S. Patent No. 5,777,610, hereinafter "*Sugimoto*").

Applicant respectfully traverses the 35 U.S.C. 103(a) rejections of claim 11 for at least the following reasons.

As stated in claim 11, "the first scanning circuit board is the same as the second scanning circuit board" and "each scanning circuit board ... comprises ... a connector ... a first scanning interface ... a second scanning interface ... and an on-board circuit."

Neither *Kinoshita* nor *Sugimoto* teach, disclose or suggest a first scanning circuit board the same as a second scanning circuit board, and each scanning circuit has a connector and two scanning interfaces. *Kinoshita* does not teach a circuit board with three connection ports, or, in other words, one connector and two scanning interfaces, as previously discussed. It is believed that, in the final office action, the Examiner refers to the connector 18 and on-board circuit (141 and 142) of *Sugimoto* as the connector and the on-board circuit in claim 11 of this application. However, one skilled in the art still cannot find two scanning interfaces in *Sugimoto*. The Examiner may interpret the places where drive ICs 16 are mounted in Fig. 4 of *Sugimoto* as scanning interfaces. Please note, however, as claimed in claim 11, any one of the scanning interfaces must transfer the scanning control signal to the scan drivers connected with the scanning interface to drive each of the scanning lines from one side of a liquid crystal display

panel. Accordingly, all the places where drive ICs 16 in one circuit board 14 of *Sugimoto*, which cause drive ICs 16 to drive each of the scanning lines from only one side of a liquid crystal display panel, are regarded as only one scanning interface in the present application. Thus, there is no second scanning interface in *Sugimoto* and *Sugimoto* fails to teach a circuit board with one connector and two scanning interfaces.

Since at least one limitation cannot be found in *Kinoshita* or *Sugimoto*, claim 11 is believed to be patentable over *Kinoshita* and *Sugimoto*.

Pending claims 13, 15, 17 and 18 are believed to be patentable since all depend from either claim 5 or 13, whose patentability is not in doubt as discussed.

Conclusion

For the reasons as described above, Applicant submits that claims 5, 11, 13, 15, 17 and 18 are allowable in their present form. Withdrawal of the rejections and allowance of the claims are respectfully requested. Applicant has made every effort to place the present application in condition for allowance. It is therefore earnestly requested that the present application, as a whole, receive favorable consideration and that all of the claims be allowed in their present form.

Should the Examiner feel that further discussion of the application and the Amendment is conducive to prosecution and allowance thereof, please do not hesitate to contact the undersigned at the address and telephone number listed below.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper may be charged to Deposit Account No. 50-2394.

Respectfully submitted,

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